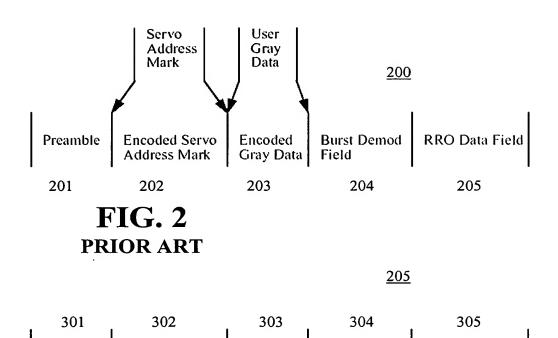
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Toggle Bit

RRO Field

RRO

Data.

RRO Parity

Field

FIG. 3
PRIOR ART

RRO

Address Mark

DC erase

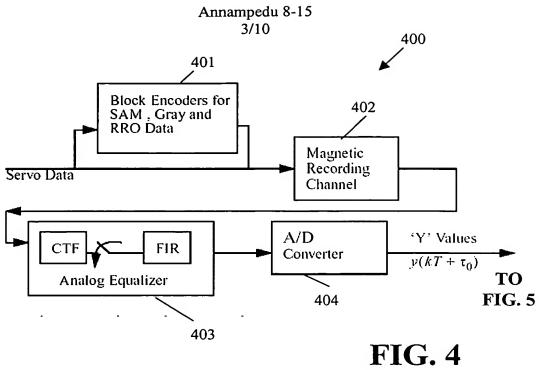


FIG. 4
PRIOR ART

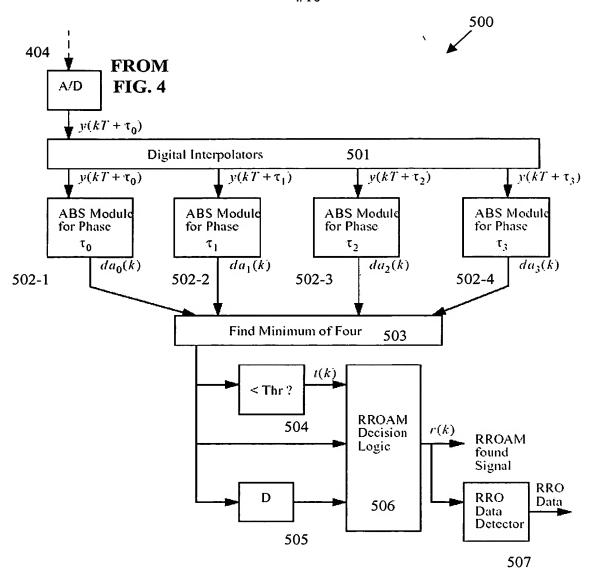
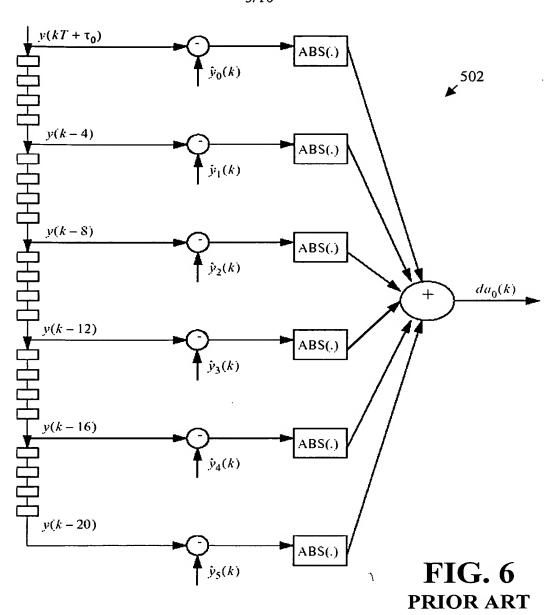


FIG. 5
PRIOR ART



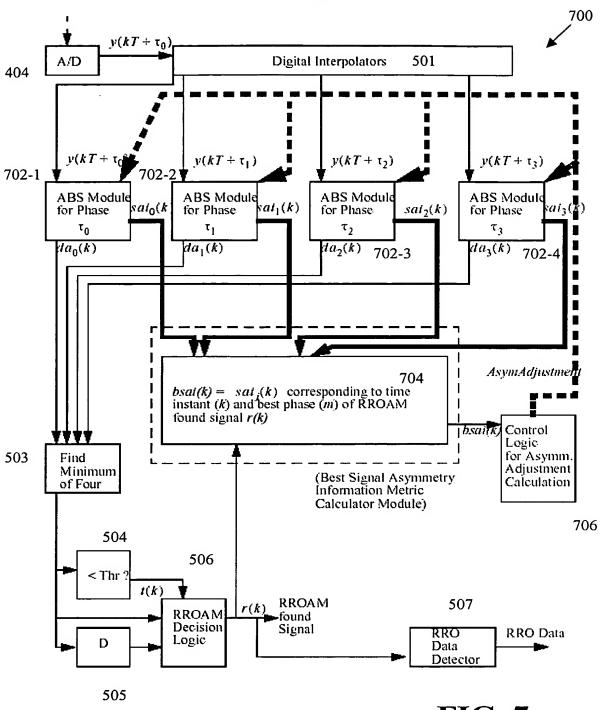


FIG. 7

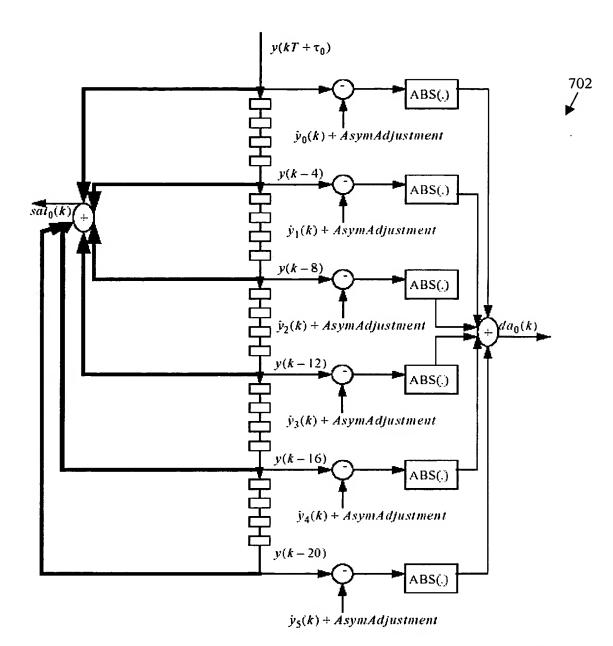


FIG. 8

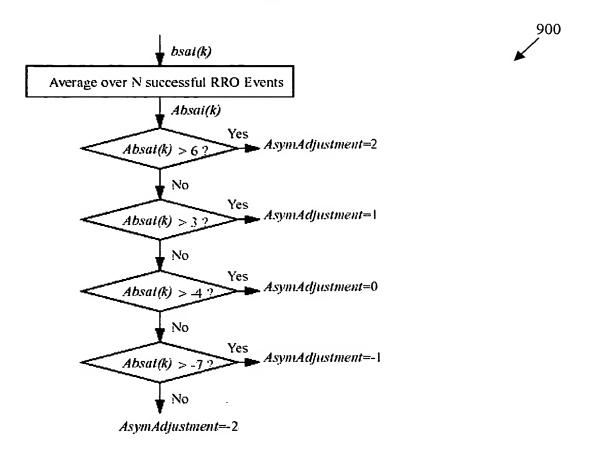


FIG. 9

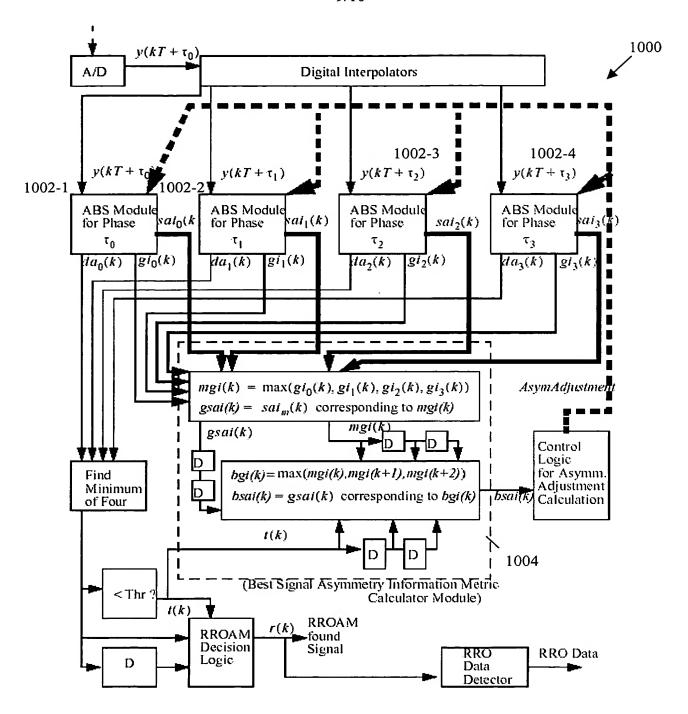
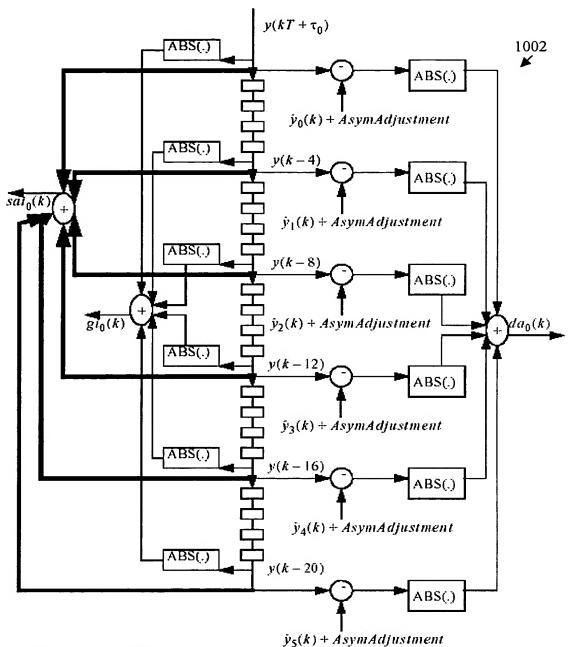


FIG. 10



Note: Refers to a Delay Element in the above figure.

FIG. 11